IN THE CLAIMS

31. (Currently Amended) A microcomputer on a semiconductor chip, the microcomputer comprising:

a central processing unit;

an electrically erasable and programmable ROM capable of storing a first program as an operation program of the central processing unit and data;

a write control circuit which performs a writing of the first program or the data to the electrically erasable and programmable ROM under control of the central processing unit;

a memory in which a second program as a write control program for writing to the electrically erasable and programmable ROM is stored; and

an input and output unit;

wherein the central processing unit performs a writing to the electrically erasable and programmable ROM of the first program input from outside of the semiconductor chip via the input and output unit by controlling the write control circuit based on the second program,

wherein the first program includes an instruction which changes a process of the central processing unit to a process that controls a writing of the electrically erasable and programmable ROM based on the second program stored in the memory, and

wherein the second program includes an instruction which returns the process of the ~~CPU~~ central processing unit to a process based on the first program stored in the electrically erasable and programmable ROM after completion of the process that controls the writing of the electrically erasable and programmable ROM~~, and~~

~~wherein significant amounts of the first program stored in the ROM are written in a write process where the central processing unit controls the write control circuit by executing the second program~~.

32. (Currently Amended) A microcomputer according the claim 31,

wherein the memory which stores the write control program is a mask ROM.

33. (Currently Amended) A microcomputer according to claim ~~32~~ 31,

wherein the memory which stores the write control program is a RAM that receives the write control program from the electrically erasable and programmable ROM.

34. (Currently Amended) A microcomputer according to claim 31, further comprising:

a data bus to which the central processing unit, the

input and output unit, the electrically erasable and programmable ROM and the memory are coupled; and

an address bus to which the central processing unit, the input and output unit, the electrically programmable and programmable ROM and the memory are coupled.